

**Abstract**

A processor resetting apparatus comprises a fibre  
channel arbitrated loop (FC-AL) interface arranged to  
5 receive a frame over the FC-AL containing an indicator  
of a reset command for a server comprising one of a  
redundant pair of servers and including a processor  
associated with the resetting apparatus. The apparatus  
further comprises a reset component, responsive to the  
10 reset command, to issue a reset command for resetting  
the processor. The apparatus therefore provides the  
ability for a server to reset another server if it  
detects that the server is faulty.

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